49 % EFFICIENCY POWER AMPLIFIER MMIC UTILIZING $SrTiO_3$ CAPACITORS FOR 3.5 V Li-ION BATTERY OPERATED CDMA CELLULAR PHONES

N. Iwata, K. Yamaguchi, T.B. Nishimura, K. Takemura[1] and Y. Miyasaka[1]

Kansai Electronics Research Laboratories, NEC Corporation
9-1, Seiran 2-Chome, Otsu, Shiga 520-0833, Japan
[1]Fundamental Research Laboratories, NEC Corporation
1-1, Miyazaki 4-Chome, Miyamae-Ku, Kawasaki, Kanagawa 216-8555, Japan

ABSTRACT

This paper describes 840 MHz IS-95 power performance of a two-stage power amplifier MMIC with 2.0×1.5 mm^2 area utilizing double-doped AlGaAs/InGaAs/AlGaAs FETs and $SrTiO_3$ capacitors. Under 3.5 V operation, the developed MMIC including input matching, inter-stage matching and bias circuits delivered an output power of 0.93 W (29.7dBm), a power-added efficiency (PAE) of 48.6 % and an associated gain of 28.4 dB with an adjacent channel leakage power of -42 dBc at 0.9 MHz off-center frequency. Even operated at a reduced supply voltage of 1.2 V, a high PAE of 46.9 % was obtained.

INTRODUCTION

In recent wireless communication systems, Code Division Multiple Access (CDMA) cellular phone systems have been introduced to further increase system capacity and data stream rate. Power amplifiers for the CDMA cellular phones are required with low distortion (e.g. IS-95 standard) as well as high efficiency characteristics over a wide range of output power level. In addition, low voltage operation with a small-sized power amplifier is essential to reduce size and weight of the handsets. However, most power devices reported are operated at 4.7 V with somewhat low efficiency [1], due to the strictness of IS-95 criteria. In this paper, a high power-added efficiency (PAE) of 48.6 % at the IS-95 criteria is described for a 3.5 V operation two-stage power amplifier MMIC utilizing double-doped AlGaAs/InGaAs/AlGaAs heterojunction FETs (HJFET) and $SrTiO_3$ (STO) capacitors.

MMIC AND ITS COMPONENTS

Figure 1 shows a cross section of the developed MMIC. The MMIC consists of a two-stage HJFET amplifier utilizing STO capacitors and spiral inductors plated with 5 μm thick Au.

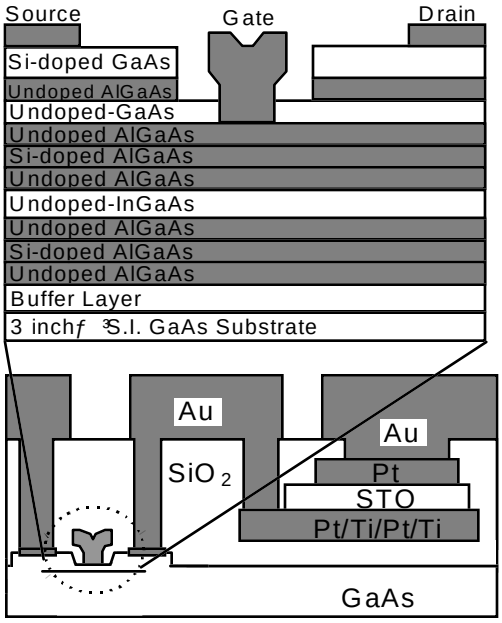

Figure 1: Cross section of the developed MMIC

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To fabricate a double recessed structure for the HJFET, electron cyclotron resonance plasma dry-etching using SF_6 and BCl_3 was employed. This enabled a remarkably small standard deviation of 20 mV for a threshold voltage of -1.1 V on a 3 inch wafer.

Figure 2 shows typical drain I-V characteristics of the HJFET. The fabricated 0.6 μm gate-length HJFET exhibited a maximum drain current of 630 mA/mm with a gate-to-drain breakdown voltage of 16.4 V. It had a low on-resistance of 2.1 Ωmm which is noteworthy as favorable for high efficiency with low distortion characteristics [2].

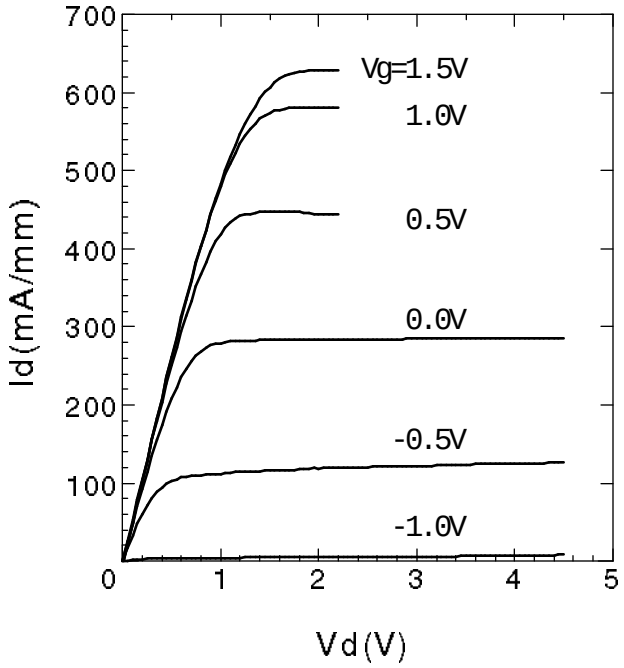


Figure 2: Drain I-V characteristics of the HJFET

The capacitor consists of a Pt/Ti/Pt/Ti base electrode, a 200 nm-thick STO film and a Pt top electrode. This multi layer base electrode has high tolerance against ion-milling for capacitor fabrication, resulting in low series resistance of the base electrode [3]. The STO film was deposited at a substrate temperature of 450 °C before the HJFET fabrication. The RF-sputtered STO capacitor exhibited a high relative dielectric constant (ε_r) of 180, thus establishing substantial reduction in the size of matching and bias circuits. This high ε_r is constant up to 20 GHz [3]. Figure 3 shows capacitance and insertion loss as a function of frequency of the fabricated STO capacitor with 2500 μm^2 area. The capacitor exhibited a low insertion loss and a high capacitance due to the low resistance of the electrodes and the high ε_r of the STO film.

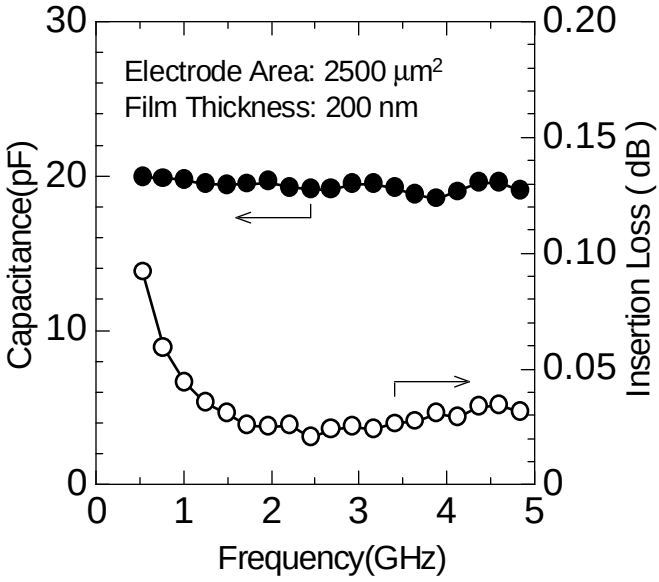


Figure 3: Capacitance and insertion loss as a function of frequency of the STO capacitor

The circuit configuration of the power amplifier MMIC is shown in Figure 4. The two-stage HJFET amplifier MMIC includes input matching, inter-stage matching and bias circuits. The gate width of the first-stage and the second-stage FETs are 4.0 and 20.0 mm, respectively.

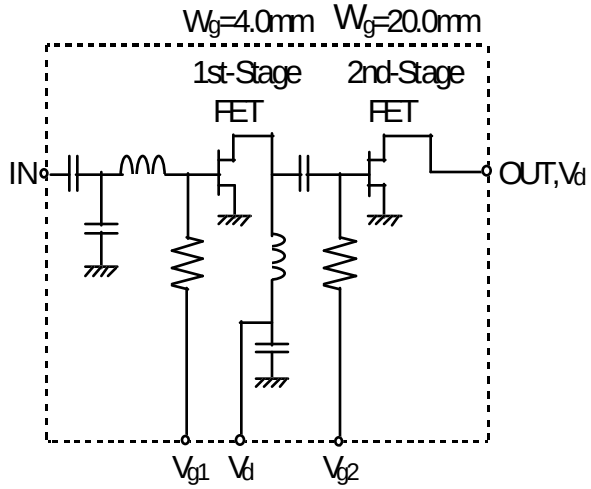


Figure 4: Circuit configuration of the MMIC

Figure 5 shows a microphotograph of the fabricated power amplifier MMIC. The chip size is as small as $2.0\times1.5\ mm^2$. High power density of the HJFET and high ε_r of STO capacitor resulted in substantial reduction in the size of MMIC.

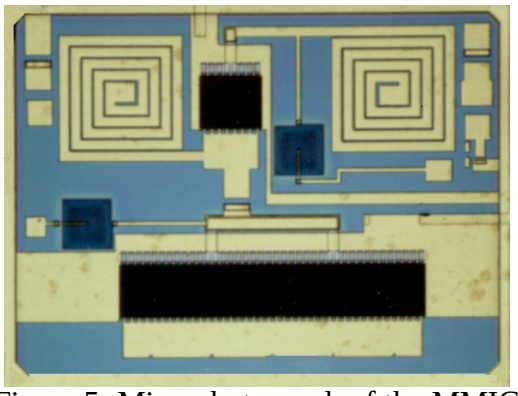


Figure 5: Microphotograph of the MMIC

RESULTS AND DISCUSSION

For IS-95 cellular applications, 840 MHz power performance of the MMIC was evaluated at a drain bias voltage (V_d) of 3.5 V. The optimum load impedance for maximum output power while maintaining low distortion characteristics was determined through load-pull measurements with a quiescent drain current of the second-stage FET (I_{q2}) of 53 mA. Figure 6 shows output power (P_{out}), PAE, gain and adjacent channel leakage power ratio at 0.9 MHz off-center frequency (ACPR(0.9MHz)) and that at 1.98 MHz off-center frequency (ACPR(1.98MHz)) as a function of input power (P_{in}) for the MMIC. The MMIC exhibited P_{out} of 0.93 W (29.7 dBm), PAE of 48.6 % and an associated gain (G_a) of 28.4 dB with ACPR (0.9MHz) of -42 dBc and ACPR(1.98MHz) of -60 dBc.

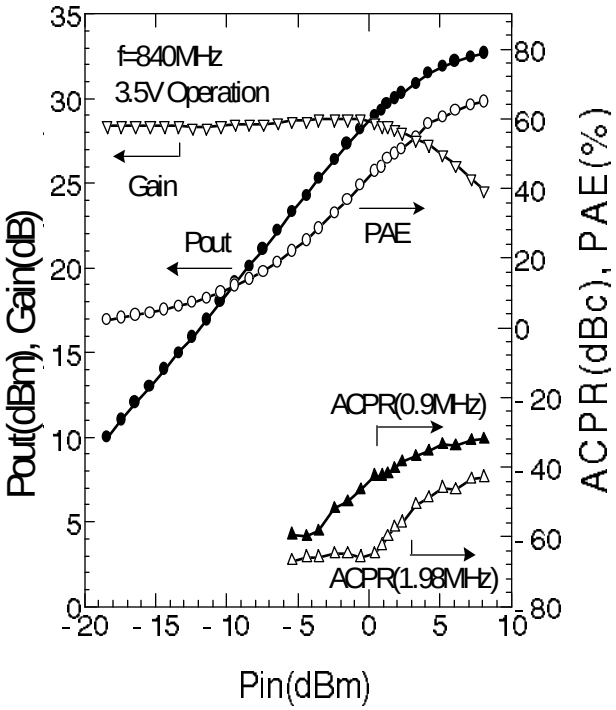
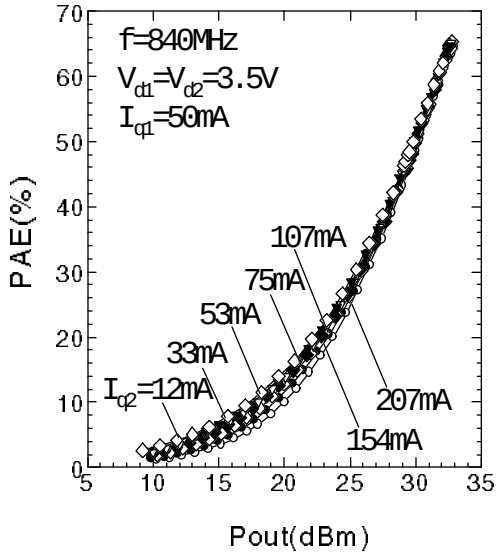
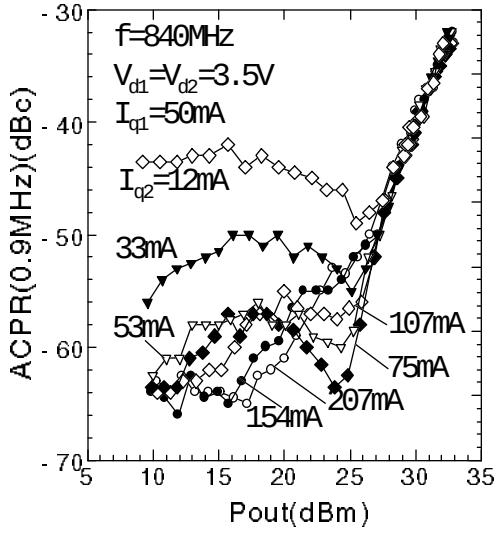


Figure 6: P_{out}, PAE, gain and ACPR as a function of P_{in} for the MMIC



a)



b)

Figure 7: a)PAE and b)ACPR(0.9MHz) vs. P_{out} for the MMIC with various I_{q2}s

The high 56.8 % drain efficiency of the second-stage FET should be emphasized. It is also notable that this high PAE of 48.6 % with 0.93 W P_{out} was achieved at V_d of 3.5 V, while a previously reported power amplifier MMIC exhibited 25 % PAE with 0.53 W P_{out} at V_d of 4.7 V [1].

The PAEs at 30 mW P_{out}, which would be a typical P_{out} for use in a city, were evaluated with various I_{q2}s. Figure 7 shows PAE and ACPR(0.9MHz) as a function of P_{out} for the power amplifier MMIC with various I_{q2}s. Under near class B operation with I_{q2} of 12 mA, a PAE of 6.5 % was obtained.

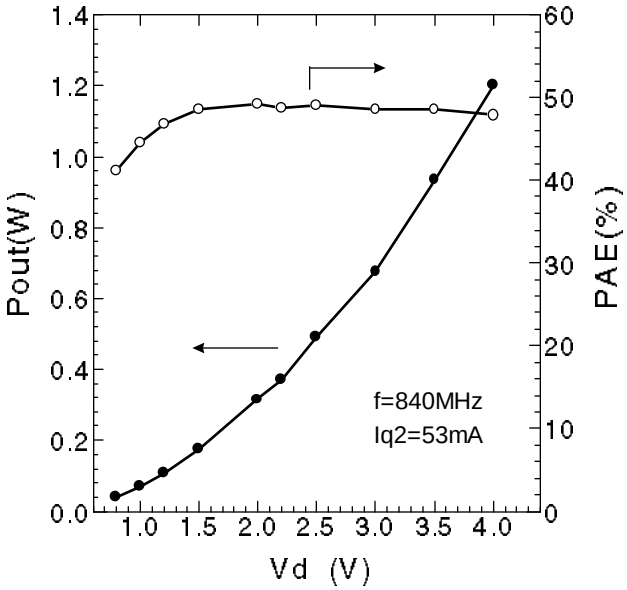


Figure 8: P_{out} and PAE as a function of V_d at ACPR(0.9MHz) of -42 dBc

The V_d dependence of CDMA power performance from 0.8 to 4.0 V with I_{q2} of 53 mA was evaluated. Figure 8 shows P_{out} and PAE as a function of V_d at ACPR(0.9MHz) of -42 dBc. The PAE exhibited flat characteristics against V_d of more than 1.2V. Even operated at the reduced V_d of 1.2 V, a high PAE of 46.9 % was achieved.

These results indicate that the developed power amplifier MMIC has great potential for small-sized light-weight CDMA cellular phones operated with one Li-Ion battery cell.

SUMMARY

A two-stage power amplifier MMIC with 2.0×1.5 mm^2 area utilizing double-doped HJFETs and STO capacitors was successfully fabricated for 840 MHz IS-95 cellular applications. Under 3.5 V operation, the MMIC including input matching, inter-stage matching and bias circuits delivered P_{out} of 0.93 W (29.7 dBm), PAE of 48.6 % and G_a of 28.4 dB with ACPR(0.9MHz) of -42 dBc. Even operated at a reduced supply voltage of 1.2 V, a high PAE of 46.9 % was obtained.

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